Amendments to the Specification:

Please amend the paragraph on page 1, lines 14-22, as follows:

The purpose of the ARL is to reduce net linewidth variations in the photolithographic process. Variations that are allowable within a 1μm or even 0.6μm process become unacceptable as devices move deeper into the submicron range. A variation of, ~~say~~**for example**, ±0.1μm or even ±0.15μm in Critical Dimension (CD) may be tolerable at 1μm, but would produce a factor of 2 or 3 difference between the upper and lower values at the 0.3μm scale. Such variations in transistor gate length can undermine device performance and reliability, particularly on the low side. An ARL layer can readily reduce such variations in CD width by a third when compared to the same process without this layer.

Please amend the two paragraphs beginning on page 3, line 17, and ending on page 4, line 2, as follows:

14. Poly oxidation for transistor and subsequent steps,

where the subsequent steps would include the standard fabrication steps, such as masking and implantation to form the transistors' source and drain, as well as any common but optional steps, such as, ~~say~~**for example**, the formation of a Lightly Doped Drain (LDD). Some of the steps on this list are themselves optional but common, such as the anneal of steps 3 and 7 or, what is more pertinent here, step 11.

This list of steps is broken into three parts. Steps 1-3 are common to both the formation of transistors for the device as well as the capacitors. If the capacitors were not needed, the process would proceed directly from step 3 to step 11 for the ARL to be applied and steps 4-10 eliminated. The inclusion of

steps 4-10 allows the fabrication of a high performance capacitor to **be** integrated into this standard CMOS process flow. In this way, these steps can be added as a group, or module, when the device being fabricated requires capacitors and otherwise deleted without changing the non-capacitor, transistor steps or flow. A variation could define and etch the lower electrode before the capacitor dielectric is formed, but it is preferred to integrate this with the etch of the standard transistor flow, particularly at 0.35μm and below.

Please amend the paragraph on page 4, lines 21-24, as follows:

The problem in this process as found in the prior **art** is in the juxtaposition of step 10 with step 11**[[:]]**. It is this combination of the dielectric removal with the application of an anti-reflective layer having poor insulation properties that is detrimental to the capacitors.

Please amend the paragraphs beginning on page 5, line 10, and ending on page 6, line 7, as follows:

This is demonstrated in Figures 10 and 11, where the solid diamonds represent this process without the ARL of step 11. Figure 10 shows cumulative probability vs. capacitor leakage current at 5 volts, with the horizontal scale logarithmic in units of $fA/\mu m^2$. For the process without an anti-reflective layer, this is a nearly vertical line at a value of $10^{-1.5} \approx 0.03 fA/\mu m^2$. Figure 11 is a plot of cumulative probability vs, capacitor voltage coefficient. This is a measure of capacitance as a function of the voltage across its plates**[[:]]**. For an idealized conducting electrode capacitor, capacitance is independent of voltage, and the graph would be a vertical line at 0. For a capacitor formed on a semiconductor device, the plates of the capacitor are now of doped silicon or similar material,

and the deviation from this ideal is measured in PPM per volt. The line should still be as vertical as possible, for device consistency, and as close to zero as possible, for the best performance of the individual capacitors. The solid diamonds of the non-ARL process are again nearly vertical, and with a magnitude of just over 20PPM/V, the negative values ~~a residue of~~**show** how the coefficient is defined. This set of points, the solid diamonds, can be seen as reference values against which a fully integrated process can be measured.

With the inclusion of both steps 10 and 11, this undercutting is now filled in by the less benign ARL. In particular, PEARL is a silicon rich Si_xON_y film and is expected to be a poor insulator, resulting in high leakage currents. This will greatly degrade both device performance, due to leakage well beyond design specifications, and stability, as variations in performance will vary over a wide voltage range of values as the amount **of** undercutting will vary from capacitor to capacitor. This is shown on Figures 10 and 11 by the solid squares. In Figure 10, these points are well to the right of the reference values with leakage currents of, at best, several orders of magnitude higher. In Figure 11, these points are far from vertical, showing a capacitance that is very voltage dependent due to excessive leakage.

Please amend the paragraph on page 7, lines 20-22, as follows:

Additional objects, advantages, and features of the present invention will become apparent ~~form~~**from** the following description of its preferred embodiments, which description should be taken in conjunction with the accompanying drawings.

Please amend the paragraph on page 12, lines 1-18, as follows:

Returning to the process flow of the preferred embodiment, in step 10a the structure of Figure 3 is subjected to a Rapid Thermal Oxidation (RTO). This involves a short oxidation in an RTO tool to grow to a layer of oxide, preferably 20Å to 60Å thick, although this could be increased to 70Å or 100Å if the extra thickness did not produce excessive degradation of the photolithographic process. This is performed for 10s to 60s at a temperature of from 850°C to 1050°C, with values in the lower part of the range preferred for minimal impact on transistor performance. The result is shown in figure 4, where the rapid thermal oxide **layer** 170 has sealed in the previous structure by filling in the undercut between the capacitor plates 140 and 120. The RTO layer **170** is left on the lower electrode during the PEARL deposition. The chosen thickness for the RTO layer **170** is a compromise: It needs to be thick enough to fill in the undercut 180, yet thin enough to not significantly degrade a photolithographic process, particularly in the transistor sector, based on previously determined parameters. At 20Å to 60Å, this is roughly an order of magnitude thinner than removed capacitor dielectric 160 and the original setting may still be successfully employed. In other embodiments, this oxide or other dielectric could be formed in a furnace or possibly even deposited with an optional anneal.

Please amend the paragraph beginning on page 14, line 17, and ending on page 15, line 2, as follows:

As described in the background section, the solid squares correspond to the prior art, while the solid diamonds are for reference and correspond to the desired result. The~~se last~~ **solid diamonds** show leakage levels when the capacitor layer is etched and the problematical PEARL ~~level~~ **layer** is absent, corresponding to the process through step 10, and produce **a** near vertical line~~s~~ at

a value of approximately $10^{-1.5} \approx 0.03 fA/\mu m^2$, well below the design objective. As discussed in the background section, this process is not preferred since the PEARL layer used in the deep submicron region is lacking. The values for the prior art (solid squares) lie well to the right of these reference values. This is a consequence of the degradation of the interpoly dielectric from the PEARL. Even when undercutting of the capacitor dielectric, indicated at 180 in Figure 3, is small, if the ARL has poor insulating properties, such as for the preferred PEARL layer, leakage between upper and lower electrodes can occur. The preferred embodiment (open circles) differs very little ~~form~~**from** the reference values, producing ~~a~~ quite vertical lines at nearly the same values in both figures 10 and 11. The alternative embodiment's values (closed circles) do not coincide as well, but still show improvement compared to the prior art.